**Remarks**

Reconsideration of pending Claims 1-34, 50-65 and 69-76 is respectfully requested.

In sum, Applicant believes that the Final Rejection is in error because:

1. The Examiner has mischaracterized the meaning of a "bond pad" as that structure is understood in the art.
2. None of (a) the alloy layer 18 of Matsunaga, (b) elements 408b with 404b and 408c with 404c of Sheu, or (c) elements 132A-132C of Duesman are structurally or functionally the same as a pad electrode (bond pad).
3. The Examiner is ignoring the single pad electrode layer **412** of Sheu.
4. The Examiner is erroneously ignoring limitations in the claims.
5. There is no motivation to modify Matsunaga to provide two bond pads, each bond pad having a *plurality* of lower metal layers.
6. The combination of Matsunaga or Sheu with the secondary references of Duesman, Ohtaka, or Geffken does not obviate the claims.
7. Matsunaga explicitly *teaches away* from applying a passivation layer over any of the center pad electrode 15a.

**Rejections under 35 U.S.C. § 102(e) (Matsunaga)**

The Examiner responded to Applicant's responsive arguments by maintaining the Section 102(e) rejection of Claims 1, 2, 5, 7-14, 16-18, 21, 28, 29, 31, 32, 34, 50, 52, 53, 55, 57-65, 69, 70, 72, 73, 75 and 76 as anticipated by USP 6,504,252 (Matsunaga). This rejection is respectfully traversed.

The Examiner maintains the rejection of the claims over Matsunaga for the following reasons (Office Action at paragraph 11 at page 19; emphasis added):

a) Matsunaga discloses bond pads formed by two metal layers — 15a, 15b, and 18 — with alloy layer (18) formed on top of pad electrodes 15a, 15b; and

b) There is no structural or functional difference between element (18) as an *alloy layer* or as a *pad electrode*.

First of all, alloy layer (18) is *not* structurally and functionally the same as a pad electrode. This is evident in the discussion of FIG. 5[1] — illustrating the probing of the pad electrodes 15a, 15b (at col. 6, lines 35-45, emphasis added):

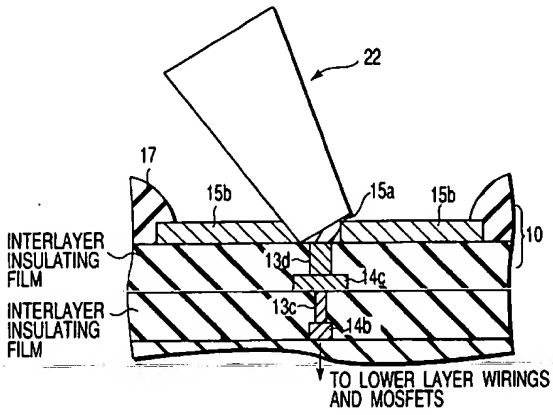



FIG. 5

> FIG. 5 shows a sectional view of the condition of the semiconductor device in which *probing is conducted on the pad electrode shown in FIG. 2.*
>
> In usual probing, *a probe 22 slides on the pad electrode 10* and breaks a natural oxide film on the surface of a material (e.g., Al) of the pad electrode 10 and intrudes thereinto. By these breaking actions, the first split pad electrode 15a is connected to the second split pad electrode 15b during probing as shown in FIG. 5. Therefore, also in probing for the evaluation of the semiconductor device, electrical connection of the pad electrode 10 can be achieved sufficiently.

In FIG. 5 —showing the probing of the pad electrodes 15a, 15b, there is *no* element (18) present as part of the pad electrode structure. Clearly, Matsunaga does not teach element (18) as part of the pad electrodes 15a, 15b.

Rather, element (18) is an alloy layer that is *only* present in the structure *in combination with the bonding wire (19)* — for attaching the wire (19) to the pad electrodes 15a, 15b — as illustrated in FIG. 3:[2]

---

[1] See the description of the drawings at col. 3, lines 64-67: " FIG. 5 is a sectional view showing the condition of a semiconductor device according to the first embodiment of the present invention with which a probe is brought into contact."

[2] Matsunaga discusses the attachment of bonding wire (19) to the pad electrodes 15a, 15b, through alloy layer (18) at col. 6, lines 10-17 (emphasis added): "FIG. 3 is a sectional view showing the condition of the semiconductor device on which bonding to the pad electrode shown in FIG. 2 is conducted...*A bonding wire 19 is bonded* onto the first and second split pad electrodes 15a and 15b, which are not covered with the passivation film 17, *through an alloy layer 18*."

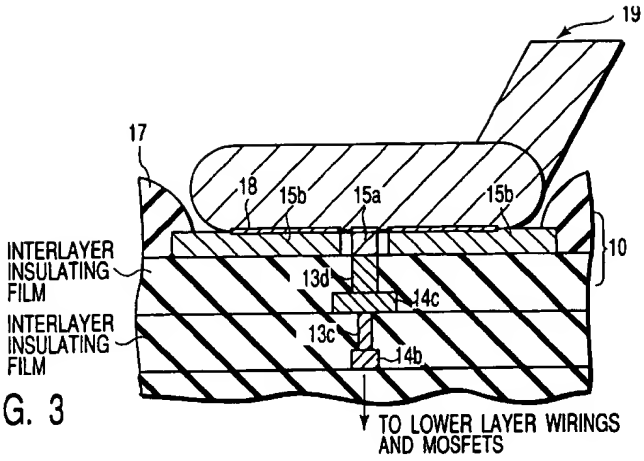



FIG. 3

Element (18) neither functions or is structurally the same as a pad electrode.

Applicant also believes that the Final Rejection is in error because Matsunaga fails to teach or suggest all of the limitations of the claims[3] — and the Examiner is erroneously ignoring the limitations in the claims.

In particular, Matsunaga fails to teach first and second bond pads — each having an upper and lower metal layer[4] — with a lower metal layer of one bond pad that extends *underneath the upper metal layer of the other of the bond pads.*

The Examiner has identified the pad electrodes 15a, 15b of Matsunaga's structure in FIG. 3 as having two metal layers — 15a with 18 and 15b with 18. As stated above, the alloy layer 18 is not part of the pad electrodes 15a, 15b. Neither layer 15a nor 15b extend beneath layer 18.

However, even accepting the Examiner's assertion as true — that the pad electrodes have two overlying layers 15a with 18 and 15b with 18 as the Examiner contends — this does not

[3] The Examiner is directed, for example, to Claim 1: A bond pad structure in a semiconductor device, comprising: a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

[4] For example, Matsunaga teaches pad electrode 15b as a "floating electrode" composed of a *single metal layer* (not an upper metal layer and a lower metal layer) — with no connections to any metal layers or wirings — in order to reduce charging damage caused from plasma processing steps in forming the pad electrodes. See cols. 1-2, bridging paragraph; col. 5, lines 36-44 and line 66 to col. 6, line 9.

meet the limitation in the claim of *a lower metal layer of one bond pad extending beneath the upper metal layer of the other of the bond pads.*

The bond pads of Applicant's semiconductor device are structured such that the lower metal layer of one of the bond pads extends beneath the upper metal layer of the other of the bond pads. The metal layers are in essence, interwoven or staggered to protect the underlying substrate. The lower metal layer of one of the bond pads forms an extension that extends beneath the upper metal layer of the other of the bond pad. Typically, an insulating passivation layer is deposited over the die and an opening is then etched to reveal the bond pads. The lower metal layer extension of the bond pad structure functions as an etch block to prevent etching of insulating material inbetween the first and second bond pads when etching the bond pad opening in the passivation layer — so that the underlying substrate is not etched or damaged during etching of the bond pad opening.

Matsunaga does not teach or suggest Applicant's bond pad structure as claimed having first and second bond pads — each bond pad having upper and lower metal layers — with a lower metal layer of one of the bond pads extending *underneath* the upper metal layer *of the other* of the bond pads.

Accordingly, withdrawal of this rejection is respectfully requested.

**Rejections under 35 U.S.C. § 102(e) (Sheu)**

The Examiner responded to Applicant's responsive arguments by maintaining the Section 102(e) rejection of Claims 22, 24, 26, 27, 71 and 74 as anticipated USP 6,455,943 (Sheu). This rejection is respectfully traversed.

The Examiner maintains the rejection of the claims over Sheu for the following reasons (Office Action at page 20, 1st paragraph; emphasis added):

a) Sheu discloses in FIG. 4 — first bond pad 408b, 404c [sic] and second bond pad 408c, 404c; and

b) There is no structural or functional difference between elements 408b with 404b, and 408c with 404c as plugs or pads.

First of all, Sheu does not disclose two bond pads as recited in the claims. The bond pad in Sheu's structure is a *single* pad electrode layer **412**, as shown in FIG. 4 below.

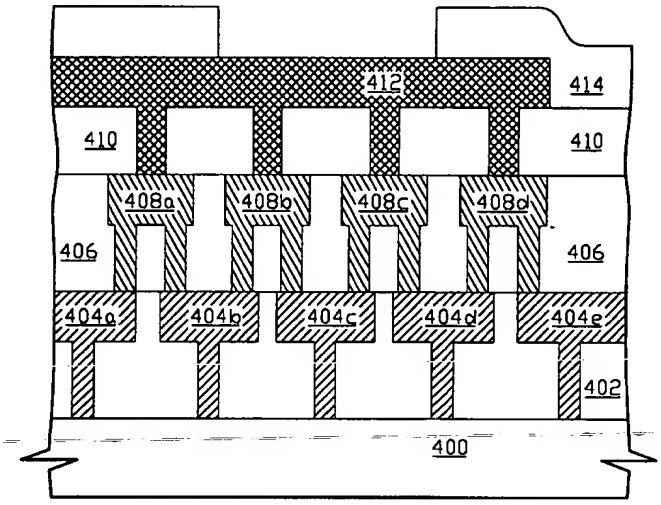



**FIG. 4**

Sheu discloses a bonding pad structure composed of a *single bonding pad layer 412* and refers separately to the islands/plugs dual damascene structure. See at col. 5, lines 39-45 (emphasis added):

> *Referring to FIG 4*, still another bonding pad structure formed by using a dual damascene process is shown... A substrate 400, dielectric layers 402, 406 and 410, dual damascene structures 404a-404e and 408a-408d, *a bonding pad layer 412*, and a passivation layer 414 *are shown in this figure*. The *bonding pad layer 412* can also be formed by...The *bonding pad layer 412* can be... The dielectric layers 402, 406 and 410 can be... The *dual damascene structure* can be... The passivation layer 414 can be...

Likewise, the claims in Sheu define the bonding pad structure as having a bonding pad layer disposed over the conductive plugs. For example, claim 1 recites a structure comprising:

> a substrate;
>
> a plurality of distributed conductive islands...;
>
> a plurality of conductive plugs on each said conductive island;
>
> a dielectric layer...; and
>
> a bonding pad layer over said dielectric layer and said conductive plugs.

The Examiner is apparently ignoring pad electrode layer **412** — and maintains that elements 408b with 404b and 408c with 404c are two "pad electrodes." The Examiner has mischaracterized the meaning of a "bond pad" as that structure is understood in the art.

The Examiner is respectfully directed to Wolf and Tauber, *Silicon Processing for the VLSI Era* (vol. 1), Lattice Press, Sunset Beach, CA (2000) at pages 827-829, which describes bonding pads as metal patterns *exposed on a chip through openings* etched into a passivation layer deposited onto a wafer surface.[5]

> **16.2.12 Passivation Layer and Pad Mask**: Finally, a *passivation* (or *overcoat*) layer...is put down onto the wafer surface...
>
> Openings are etched into this layer so that a set of special metallization patterns under the passivation layer is exposed. These metal patterns are normally located in the periphery of the circuit and are called *bonding pads* (FIG. 16-20)...Wires are connected (bonded) to the metal of the bonding pads and then bonded to the chip package...

Similarly, Sheu discloses a *single* pad electrode layer **412** that is exposed through an opening in the passivation layer 414.

As Wolf and Tauber describe, wires are bonded to the exposed surface of the bonding pads. Likewise, in describing the related art, Sheu also discloses that bond pads are exposed on the chip to facilitate the bonding of wires from the chip's bonding pads to an external device (see at col. 1, lines 17-20 and 47-50):

> ...Electrical connections between integrated circuits on a chip and the printed circuit board are made through bonding pads typically provided at the periphery of the chip...
>
> ...Electrical connections between the bonding pads of the chip and the circuit board on which the chip is mounted are typically provided by wire bonding thin wires between the chips bonding pads and the leads printed on the board.

Elements 408b with 404b and 408c with 404c — are not structurally or functionally the same as two bond pads. These elements are not exposed for electrical connection to an external device. These elements are beneath the surface of the device. Rather, the bond pad structure in Sheu's device is a *single* bonding pad layer **412**, which is exposed through an opening in the passivation layer 414.

---

[5] See also, Stanley Wolf, *Silicon Processing for the VLSI Era* (vol. 2), Lattice Press, Sunset Beach, CA (1990) at page 377. See also Peter Van Zant, *Microchip Fabrication*, 4th ed., McGraw-Hill, New York, NY (2000): at pages 82-83 illustrating bonding pads (3) on a chip; at page 560: "...the chip wiring terminates in the larger bonding pads around the edge of the chip;" and the definition of "bonding pads" at page 596:

> **bonding pads** Electrical terminals on the chip (generally around the periphery) used for connection to the package electrical system.

Sheu does not teach or suggest Applicant's bond pad structure as claimed having first and second bond pads — with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads. Accordingly, withdrawal of this rejection is respectfully requested.

**Rejections under 35 U.S.C. §103(a)**

The Examiner maintains the Section 103(a) rejections of Claims 3, 4, 30, 33, 51 and 56 as obvious over Matsunaga in view of USP 6,078,100 (Duesman); Claims 6, 15, 20 and 54 as obvious over Matsunaga in view of USP 6,509,643 (Ohtaka); Claim 19 as obvious over Matsunaga; Claim 23 as obvious over Sheu in view of USP 5,883,435 (Geffken); and Claim 25 as obvious over Sheu in view of Ohtaka. These rejections are respectfully traversed.

The Examiner maintains the obviousness rejections of the claims for the following reasons (Office Action at pages 20-21; emphasis added):

a) in Duesman, there is no structural or functional difference between elements 132A-132C as internal traces or bonding pads (re. claims 3, 4, 30, 33, 51, 56);

b) the only reliance on Ohtaka is the use of a solder material as the conductive material, and it is irrelevant that Ohtaka does not teach or suggest connecting two bond pads with a conductive material (re. claims 6, 15, 20 54; and claim 25);

c) an art worker would be motivated by Matsunaga to overlie each of the split pad electrodes 15a, 15b with a passivation layer — based on "the knowledge generally available to one of ordinary skill in the art such as preventing the bond pads from peeling" (re. claim 19[6]); and

d) Sheu discloses in FIG. 4 — two layers of bond pad (408a and 404c), and a combined structure of Geffken and Sheu discloses the bond pad structure of claim 23.

[6] Claim 19: The bond pad structure of Claim 18, further comprising a passivation layer overlying a portion of each of the bond pads, the opening being formed through the passivation layer to expose the bond pads.

Rejection of Claims 3, 4, 30, 33, 51 and 56 as obvious over Matsunaga in view of Duesman.

The Examiner maintains the rejection of the claims over Matsunaga combined with Duesman on the basis that:

a) it would be obvious to modify Matsunaga by using the plurality of lower metal layers as taught by Duesman in FIG. 4a, and

b) there is no structural or functional difference between elements 132A-132C as internal traces or bonding pads.

First of all, contrary to the Examiner assertion —elements 132A-132C of Duesman are *not* structurally or functionally the same as bond pads.[7] These elements are not exposed for electrical connection to an external device. These elements are beneath the surface of the device.[8]

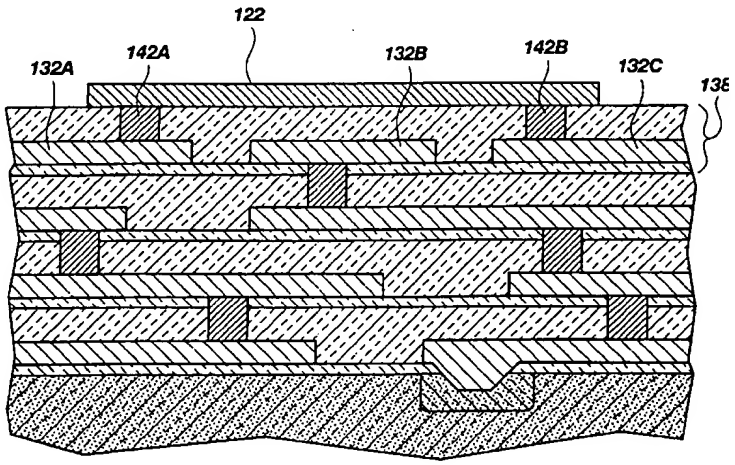



*Fig. 4a*

Furthermore, there is no motivation in either reference to modify Matsunaga to provide two bond pads — *each* bond pad having a *plurality* of lower metal layers.

A stated objective of Matsunaga is to decrease charging damage to the pad electrode that can result from various plasma processing steps (see cols. 1-2, bridging paragraph).

---

[7] See the discussion above regarding "bonding pads," and the enclosed pages from Wolf and Tauber (2000), Wolf (1990), and Van Zant (2000).

[8] It is also noted that element (122) in FIG. 4a is a routing trace ("jumping" trace) for circuitry within the flip-chip 100 — not a bonding pad. See FIG. 3 and cols. 4-5, bridging paragraph, and col. 5, lines 35-45.

To that end, Matsunaga clearly and particularly teaches a split pad electrode in which a first pad electrode 15a is connected to wirings and a second pad electrode 15b is a *floating electrode* that is not connected to wirings. See FIG. 2 and the discussion at col. 5, lines 36-44 and line 66 to col. 6, line 9 (emphasis added):

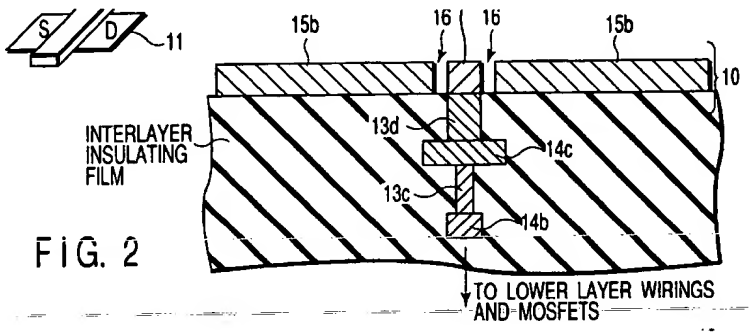



FIG. 2

> A first embodiment shows a structure which is a base of the present invention. *The present invention is characterized by the fact that a pad electrode* for probing or connection to a connecting member such as a bonding wire and a bump *is split into* a part electrode which is electrically connected to wirings and semiconductor elements ***and a part electrode which is not electrically connected to wirings and semiconductor elements***.
>
> ...
>
> As outlined above, the pad electrode 10 used in the present invention comprises the first split pad electrode 15a disposed in the center and the second split pad electrode 15b disposed apart from the first split pad electrode 15a so as to surround the first split pad electrode 15a. The first split pad electrode 15a is connected to the wirings 14a, 14b and 14c and to the MOSFET 11 in the semiconductor device ***whereas the second split pad electrode 15b is not connected to the wirings*** *14a, 14b and 14c and to the MOSFET 11* in the semiconductor device. ***Namely, the second split pad electrode 15b is made to be a floating electrode***.

The split electrode structure of Matsunaga in which the second pad electrode 15b is not connected to any wiring is a key element of Matsunaga's invention — by decreasing the area which is a charge introduction port in plasma processing steps and thus preventing damage to the device. See, for example, col. 2, lines 24-42, and col. 3, lines 25-35.

Based on the explicit teachings of Matsunaga of a floating pad electrode that is not connected to any secondary metal layers, there is no motivation to modify Matsunaga as proposed.

Accordingly, withdrawal of the rejection of Claims 3, 4, 30, 33, 51 and 56 is respectfully requested.

Rejection of Claims 6, 15, 20 and 54 as obvious over Matsunaga in view of Ohtaka, and Claim 25 as obvious over Sheu in view of Ohtaka.

The Examiner maintains the rejection of the claims over Matsunaga or Sheu combined with Ohtaka on the basis that it would be obvious:

a) to modify Matsunaga or Sheu by interconnecting the first bond pad to the second bond pad with a conductive material;[9] and

b) to use a conductive material comprising a solder material (based on Ohtaka).

As stated above, Matsunaga does not teach or suggest a bond pad structure having first and second bond pads — each bond pad having upper and lower metal layers — with a lower metal layer of one of the bond pads extending *underneath* the upper metal layer *of the other* of the bond pads.[10]

Accordingly, even if, *arguendo*, one were to utilize a solder material based on Ohtaka to connect the pad electrodes 15a, 15b of Matsunaga, this would not arrive at Applicant's device as recited in Claims 6, 15, 20 and 54.

As for Sheu, as previously stated, Sheu teaches a *single bond pad* **412** — not two bond pads as claimed by Applicant.[11] As such, there is no need for any interconnection between bond pads in Sheu's structure. Thus, the disclosure of Ohtaka combined with that of Sheu does not teach or suggest the bond pad structure recited in Claim 25.

Accordingly, withdrawal of the rejection of Claims 6, 15, 20 and 54, and Claim 25 is respectfully requested.

Rejection of Claim 19 based on Matsunaga.

The Examiner maintains the rejection of Claim 19 over Matsunaga on the basis that an art worker would be motivated to overlie *each* of the pad electrodes 15a, 15b with a passivation layer.

---

[9] Claim 6 depends from Claim 5 which recites: "The bond pad structure of Claim 1, further comprising a conductive material interconnecting the first bond pad to the second bond pad."

[10] See above discussion under Section 102(e) rejection of claims based on Matsunaga.

[11] See above discussion of Section 102(e) rejection of claims based on Sheu. The Examiner has apparently ignored the single pad electrode layer 412, and has misconstrued underlying elements 408b/404b and 408c/404c as "pad electrodes." The understanding in the art – as demonstrated by the enclosed references, does not support the Examiner's interpretation.

First of all, the Examiner has provided no good basis for forming a passivation layer over both of the pad electrodes 15a, 15b in Matsunaga. The Examiner states that the motivation is based on "knowledge generally available to one of ordinary skill in the art such as preventing the bond pads from peeling."

The only reference to "peeling" in Matsunaga is at col. 1, lines 56-67, with reference to "peeling off a resist" after a bond pad opening is etched in the passivation film (emphasis added):

> However, as aforementioned, a relatively large area is required for the pad electrode 100 to allow wire bonding and bump connection. ... a step of depositing a passivation film on the pad electrode 100, an etching step for opening a pad window *and a step of peeling off a resist after the pad window is opened*. ...

Furthermore, Matsunaga explicitly *teaches away* from applying a passivation layer over any of the center pad electrode 15a. Matsunaga particularly states that applying a passivation layer to cover the clearance (slot) 16 between the center pad electrode 15a and the outer pad electrode 15b can *impair bonding* (at cols. 6-7, bridging paragraph, emphasis added):

> In the meantime, generally, when a pad electrode is split, a clearance is formed between the split pad electrodes and the side surface of the split pad electrode is exposed. If this side surface is brought into contact directly with a resin for sealing a semiconductor device, there is the case where the pad electrode is corroded from the exposed side surface of the pad electrode by, for example, the interaction between the water intruded from the outside through this resin and ionic impurities in the resin. For this, in order to prevent the corrosion of the exposed side surface of the pad electrode, there is the idea that the clearance between the split pad electrodes is covered with a passivation film. In this case, the surface of each of the split pad electrodes is exposed from each different opening formed in the passivation film. ***However, the passivation film covering the clearance is sometimes broken during bonding and its residue causes the durability during bonding to be impaired.***

Matsunaga solves this problem by completely covering the clearance 16 between the split pads 15a, 15b with a *bonding wire* and *eliminating the passivation layer* over the clearance between the two pads (at col. 7, lines 15-39, emphasis added):

> In the first embodiment, on the other hand, as to the condition after the bonding is finished as shown in FIG. 3 and FIG. 4, bonding can be carried out such that the contact surface between both the bonding wire and the bump and the pad electrode 10 surrounds the inner periphery of the second split pad electrode 15b disposed so as to surround the island-like first split pad electrode 15a. ***Therefore, the clearance 16 between the first split pad electrode 15a and the second split pad electrode 15b can be completely covered with the bonding wire and the bump and the side surface of each of the first and second split pad electrodes 15a and 15b is not exposed.*** The surface of each of the first and second split pad electrodes 15a and 15b is exposed from one opening of the passivation film 17 covering the peripheral part of the second split pad electrode 15b ***and the passivation film is not formed so as to cover the clearance splitting the pad***

***electrode and this makes it possible to be free from the problem that the durability during bonding is impaired.*** ....

The Examiner's assertion that one would be motivated to apply a passivation layer over both pad electrodes 15a, 15b of Matsunaga is clearly without basis, and directly opposite to Matsunaga's disclosure.

The Examiner's rejection of Claim 19 based on the proposed modification of Matsunaga is clearly without merit and should be withdrawn.

Rejection of Claim 23 as obvious over Sheu in view of Geffken.

The Examiner maintains the rejection of Claim 23 over Sheu combined with Geffken on the basis that:

a) Sheu discloses in FIG. 4 — two layers of bond pad (408a and 404c), and

b) a combined structure of Geffken and Sheu discloses the bond pad structure of Claim 23.[12]

The Examiner cites Geffken as disclosing in FIG. 5 — a passivation layer 130 formed over bond pads 126, 128 and etched to form an opening 150 to exposed the bond pads.

First of all, as stated above, Sheu does not disclose two bond pads as recited in the claims. The bond pad in Sheu's structure is a *single* pad electrode layer **412** (see FIG. 4 above).[13]

Further, as previously stated — *Sheu* discloses a passivation layer **414** formed over pad electrode 412 with an opening that exposes the *single* pad electrode **412** (see FIG. 4 above).

Likewise, Geffken discloses openings 150 in a passivation layer 130 to expose contacts 126, 128.

The disclosure of Geffken combined with Sheu does not teach or suggest the bond pad structure recited in Claim 23.

Sheu — either along or combined with the disclosure in Geffken —does not teach or suggest Applicant's bond pad structure as claimed having first and second bond pads — with a

[12] Claim 23: The bond pad structure of Claim 22, further comprising a passivation layer formed over the bond pads and etched to form an opening therethrough to expose the first and second bond pads.

[13] See above discussion under Section 102(e) rejection of claims based on Sheu. As argued, the Examiner is apparently ignoring pad electrode layer **412** — and maintains that elements 408b with 404b and 408c with 404c are two "pad electrodes." The Examiner has mischaracterized the meaning of a bond pad as that structure is understood in the art.

lower metal layer portion of one of the bond pads extending beneath the upper metal layer portion of the other of the bond pads. Accordingly, withdrawal of this rejection is respectfully requested.

In sum, neither Matsunaga nor Sheu, either alone or combined with the secondary references of Duesman, Ohtaka and/or Geffken, teach or suggest Applicant's bond pad structure as claimed. Accordingly, withdrawal of these rejections is respectfully requested.

**Extension of Term.** The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time.

Based on the above remarks, the Examiner is again respectfully requested to reconsider and withdraw the rejections of the claims.

Respectfully submitted,

Kristine M Strodthoff

Dated: October 16, 2003

Kristine M. Strodthoff
Reg. No. 34,259

WHYTE HIRSCHBOECK DUDEK S.C.
111 East Wisconsin Avenue, Suite 2100
Milwaukee, Wisconsin 53202
(414) 273-2100

Customer No. 31870

# SILICON PROCESSING FOR THE VLSI ERA

## VOLUME 1:

## PROCESS TECHNOLOGY

Second Edition

STANLEY WOLF Ph.D.

RICHARD N. TAUBER Ph.D.

LATTICE PRESS

Sunset Beach, California

DISCLAIMER

This publication is based on sources and information believed to be reliable, but the authors and Lattice Press disclaim any warranty or liability based on or relating to the contents of this publication.

Published by:

**LATTICE PRESS**
Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon, New Archetype Publishing, Los Angeles, CA.



**Library of Congress Cataloging in Publication Data**
Wolf, Stanley and Tauber, Richard N.

Silicon Processing for the VLSI Era
Volume 1: Process Technology

Includes Index
1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

ISBN 0-9616721-6-1

9 8 7 6 5 4 3 2 1

PRINTED IN THE UNITED STATES OF AMERICA

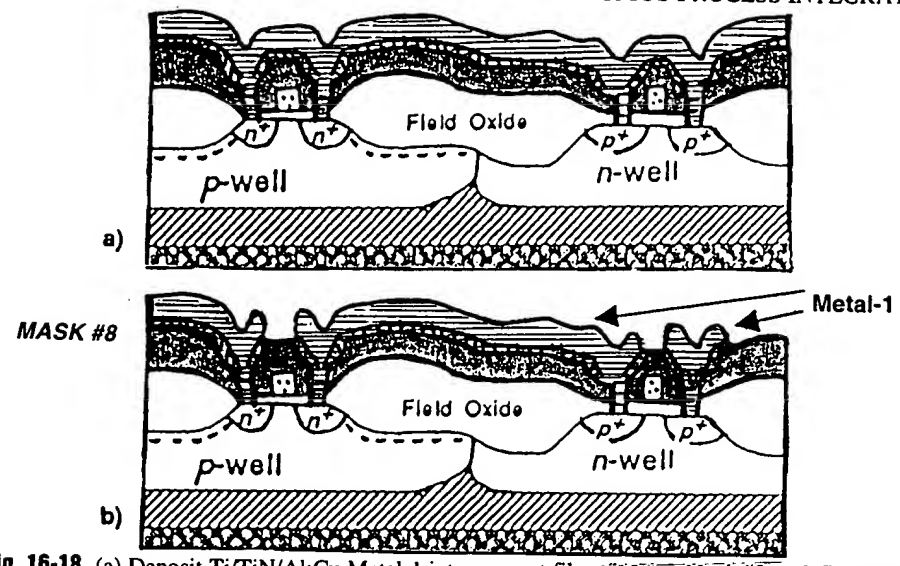



**Fig. 16-18** (a) Deposit Ti/TiN/Al:Cu-Metal-1 interconnect film. (b) Use *Mask #8* to define Metal-1 pattern and then etch the metal with a dry-etch process.

establishes a low-resistance ohmic contact. The annealing process exposes the wafer to a 375–500°C temperature in an $H_2$, or $N_2 + H_2$ (5%) ambient for about 30 minutes. This step is also used as the annealing process for reducing the interface trap density in the gate oxide that was introduced by earlier processing steps (see Chap. 8).

**16.2.10 Intermetal Dielectric Deposition and Via Patterning:** If a two-level-metal interconnect structure is used, an *intermetal dielectric* (*IMD*) must be deposited to electrically isolate the Metal-1 layer from the Metal-2 layer (Fig. 16-19a). A variety of CVD processes for depositing such dielectric films have been developed (see Chap. 6).

Deposition of this layer may make the wafer topography once again too severe to allow Metal-2 films to be deposited with adequate step coverage. One of the planarization processes discussed in Chap. 15 may need to be used to overcome this difficulty.

If such techniques are successfully implemented, the wafer topography will be relatively planar, and any steps on its surface will be gently sloped rather than severely vertical. It is also necessary to open vias in the intermetal dielectric layer so an electrical connection can be established between Metal-2 and Metal-1 at desired locations (*Mask #9*). Metal-2 must be deposited with adequate step coverage into these vias, but reflow is not possible because Al is present on the wafer (Metal-1). Thus, in this example, a champagne glass etch process is again used to etch the vias (Fig. 16-19b).

**16.2.11 Metal 2 Deposition and Patterning.:** The processing issues of depositing and patterning (*Mask #10*) the Metal-2 layer (Fig. 16-19c) are discussed in Chaps. 11, 14, and 15.

**16.2.12 Passivation Layer and Pad Mask:** Finally, a *passivation* (or *overcoat*) layer, such as CVD PSG or plasma-enhanced CVD silicon nitride (or both), is put down onto the wafer surface (Fig. 16-19d). This layer seals the device structures on the wafer, protecting them from contaminants and moisture. It also serves as a scratch protection layer.

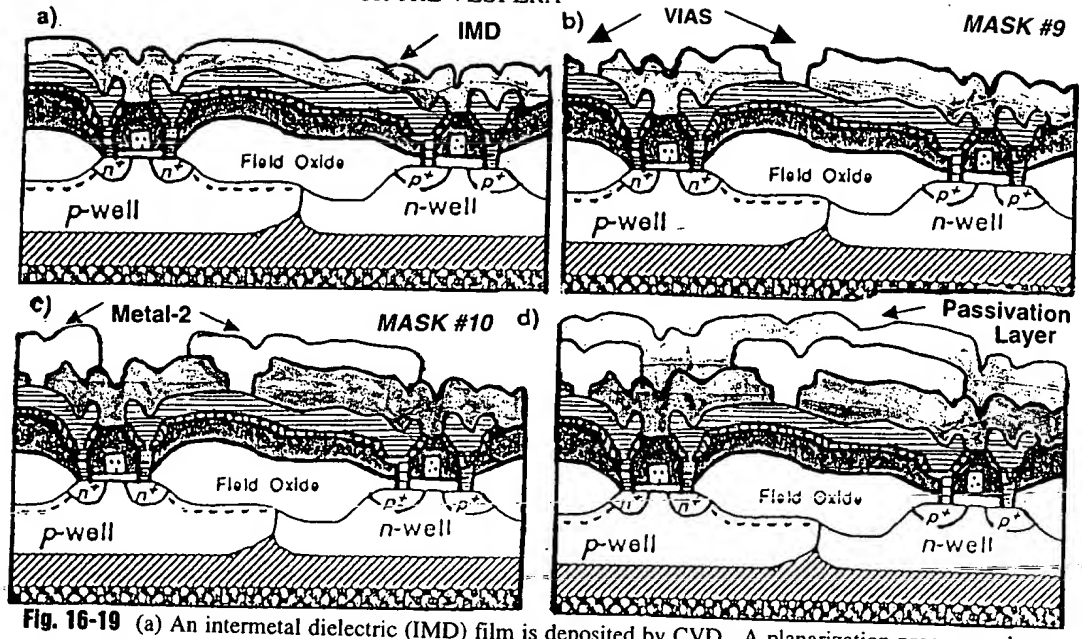



**Fig. 16-19** (a) An intermetal dielectric (IMD) film is deposited by CVD. A planarization process such as resist etchback, or spin-on-glass, may be used to smooth this surface. (b) Vias are defined in the IMD film with *Mask #9* and an etch step. (c) Metal-2 is deposited and defined with *Mask #10* and a metal etch process. (d) A final passivation layer is deposited on the wafer by CVD.

Openings are etched into this layer so that a set of special metallization patterns under the passivation layer is exposed. These metal patterns are normally located in the periphery of the circuit and are called *bonding pads* (Fig. 16-20). Bonding pads are typically about 100 x 100 $\mu$m in size and are separated by a space of 50 to 100 $\mu$m. Wires are connected (bonded) to the metal of the bonding pads and are then bonded to the chip package. In this way connections are estab-

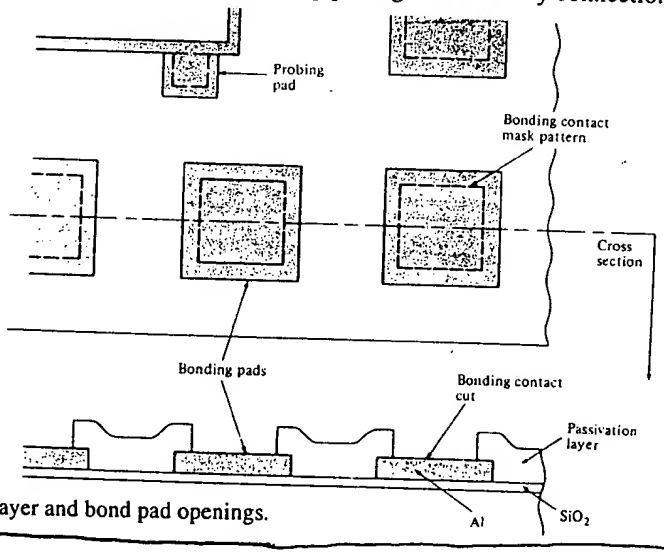



**Fig. 16-20** Passivation layer and bond pad openings.

lished from the chip to the package leads (see Chap. 17 for details on chip bonding).

The bond pad openings are created by patterning the passivation layer with *Mask #11*. If a PSG layer is used, the phosphorus (2-6 wt%) in the glass not only causes it to act as a getter for Na but also prevents the film from cracking. Care must be taken to ensure that not more than 6% phosphorus is incorporated into the PSG, as this can cause corrosion of the underlying metal if moisture enters the circuit package (see Chap. 11). When silicon nitride is used, care must be taken to ensure that the deposited nitride film exhibits low stress (either tensile or compressive), so it will not crack. Cracking would compromise the sealing capability of the film.

## 16.3 PROCESS FLOW FOR 0.25 μm CMOS

An example process flow for 0.25 μm CMOS (and perhaps for the 0.18 μm generation as well) will be presented in this section. (At this book's writing, the process flows for 0.25 μm CMOS, and below, were not yet "standardized," and many possible variations of the flow postulated here existed.) This flow is "compiled" from the literature, where a number of 0.25 μm CMOS technologies are reported, including those in Refs. 11, 12, 13, 14. Since the literature does not provide all the details of such flows, some of the information here is necessarily conjectural. Despite these issues, the 0.25 μm flow presented here should be a reasonable representation of those found in actual use.

A number of general characteristics of 0.25 μm CMOS process technology should be noted. First, the lithography technology used for the critical masking layers is DUV optical lithography, which is based on 248-nm KrF laser light sources (and *i*-line lithography perhaps being used for the non-critical layers). Second, the power supply voltages of the systems using 0.25 μm CMOS is 2.5 V, and for 0.18 μm CMOS is estimated to be 1.8 V. This is a deviation from the 5-V power supply used from the mid-1970s's and down to when CMOS reached 0.65 μm. However, when CMOS reached 0.5 μm, the gate oxide thickness had been scaled so much that the electric field across the gate oxide exceeded the value that would permit reliable operation for the designed life of the systems (e.g., 10 years). To ensure adequate device lifetime, the power supply voltage had to be changed for 0.5-μm CMOS to 3.3 V, and again at 0.25-μm CMOS to 2.5 V. (This is an example of how the limits of process technology impact the electronic systems specifications.) Third, the number of masking layers is likely to exceed 20, especially if 5 or more interconnect levels are needed. Finally, 0.25-μm CMOS was initially being manufactured on 200-mm wafers. It is likely that 0.18-μm CMOS will also use such wafer sizes. However, it appears that 0.15-μm CMOS, or 0.12-μm CMOS will enter large scale production on 300-mm wafers.

As mentioned in the introduction, there are a number of process modules that had to be fundamentally changed as CMOS technology was scaled below about 0.35 μm. Figure 16-21 demonstrates this quite clearly.[13] The order of carrying out some of the steps has also changed. Why these changes in the process flow were necessary will be indicated.

**16.3.1 Starting Material:** The starting material for deep-submicron CMOS is predicted to shift more to $p$-epi-on-$p^+$ wafers (Fig. 16-7b), because the gate-oxide-integrity is better on epi than on bulk wafers. However, the higher cost of epi compared to bulk wafers remains a concern, especially for such low-price commodity chips as DRAMs. Less expensive alternatives to epi are being studied. One process that shows great promise is the implantation of a high dose of

is placed on the hot adhesive with a force of 150–200 grams for up to two minutes at a temperature of 230°C. The thermoplastic nature makes this adhesive amenable to remelting for hybrid circuit repair or rework, but it also limits the maximum wire bonding temperature. That is, a 220°C maximum thermosonic wire-bonding temperature limit is recommended.

### 17.4.3 Die Attach Equipment

Equipment used in the process of die attach has evolved from operator controlled manual systems to the fully-automatic systems in standard use today. Systems capable of die bonding up to 4000 to 6000 parts/hr are now available, particularly for epoxy attachment. In such die bonders the wafers are presented in sawed-wafer form attached to an adhesive Mylar tape. The die-bonder has a pick-and-place unit, and the pickup arm then moves into position over the die to be attached. The arm is lowered so that a vacuum collet can pickup the die (Fig. 17-6). At the same time that the collet lifts the die, an ejector needle pushes the die from underneath, causing the die and the adhesive Mylar tape to disengage from one another. Some collet designs make contact with the upper edges of the die, while others have a rubber tip that makes contact only with the top surface of the die as it is lifted. Pattern recognition systems enable the machines to recognize chipped die or rejected die. The die to be bonded is then placed on the package substrate, onto which has previously been placed the die-attach material. Die placement pressure is applied by the bond arm, and can be programmed to accommodate different die sizes. The die-bonder also contains a chip-attach material supply station and a lead-frame loader and unloader.

Automatic die bonders must have the following characteristics. First they must perform the die attach process for a variety of applications. For example, new package types are continually being developed, especially to accommodate large die. Thus, the equipment may need to handle a wide range of die sizes. Second, the yield of the die-attach process must be high, and the long term reliability of the bonded parts must also be preserved. Third, the equipment must operate with a reliability of more than 90% uptime. Fourth, the equipment should be flexible enough to accommodate a wide range of product types, and be able to be converted quickly from one product type to another. Finally, the equipment needs to be easily integrated into a computer-controlled factory-automation system. Die bonders in 1999 ranged from $80,000–$250,000 for fully automated systems.

## 17.5 BOND-PAD TO PACKAGE CONNECTIONS

After the chip has been attached to the package substrate (or leadframe), electrical connections must be made between the bonding pads of the chip and the inner leads of the package (which are themselves connected to the package pins).[7] Wire bonding has been, and will likely remain, the most common technique for making the connections between the chip input/outputs (I/Os) and the package (especially for chips with up to about 224 I/Os). It is estimated that in 1996 over $4 \times 10^{12}$ wire bonds were formed in the fabrication of ICs. In this section wire bonding is discussed first. The other two methods for making such connections are tape-automated bonding (TAB), and flip-chip bonding. They are discussed in subsequent sections.

### 17.5.1 Wire Bonding

The wire bonding process is carried out after the die-attach step. Flexible wires are attached, one at a time, from bonding pads on top of the chip to the package. One of three methods is used to

# SILICON PROCESSING

# FOR

# THE VLSI ERA

## VOLUME 2:

## PROCESS INTEGRATION

**STANLEY WOLF Ph.D.**
Professor, Department of Electrical Engineering
California State University, Long Beach
Long Beach, California

**LATTICE PRESS**

Sunset Beach, California

DISCLAIMER

This publication is based on sources and information believed to be reliable, but the authors and Lattice Press disclaim any warranty or liability based on or relating to the contents of this publication.

Published by:

Lattice Press,
Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon, Visionary Art Resources, Inc., Santa Ana, CA.



Library of Congress Cataloging in Publication Data
Wolf, Stanley

Silicon Processing for the VLSI Era
Volume 1 : Process Integration

Includes Index
1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

86-081923

ISBN 0-961672-4-5

9 8 7 6

PRINTED IN THE UNITED STATES OF AMERICA

$N_2 + H_2$ (5%) ambient for about 30 minutes. As a result, this step may also be used as the annealing process for reducing the interface trap density in the gate oxide that was introduced by earlier processing steps (see Vol. 1, chap. 7).

**5.4.1.8 Passivation Layer and Pad Mask.** Finally, a *passivation* (or *overcoat*) layer, such as CVD PSG or plasma-enhanced CVD silicon nitride, is put down onto the wafer surface. This layer seals the device structures on the wafer from contaminants and moisture, and also serves as a scratch protection layer.

Openings are etched into this layer so that a set of special metallization patterns under the passivation layer is exposed. These metal patterns are normally located in the periphery of the circuit and are called *bonding pads* (Fig. 5-16). Bonding pads are typically about 100 x 100 $\mu$m in size and are separated by a space of 50 to 100 $\mu$m. Wires are connected (bonded) to the metal of the bonding pads and are then bonded to the chip package. In this way connections are established from the chip to the package leads.

The bonding-pad openings are created by patterning the passivation layer with *Mask #7*. If a PSG layer is used, the phosphorus (2-6 wt%) in the glass not only causes the PSG to act as a getter for Na but also prevents the glass film from cracking. Care must be taken to ensure that not more than 6% phosphorus is incorporated into the PSG, as this can cause corrosion of the underlying metal if moisture enters the circuit package (see Vol. 1, chap. 10). When silicon nitride is used, care must be taken to ensure that the deposited nitride film exhibits low stress (either tensile or compressive), so that it will not crack, since cracking would compromise the sealing capability of the film.

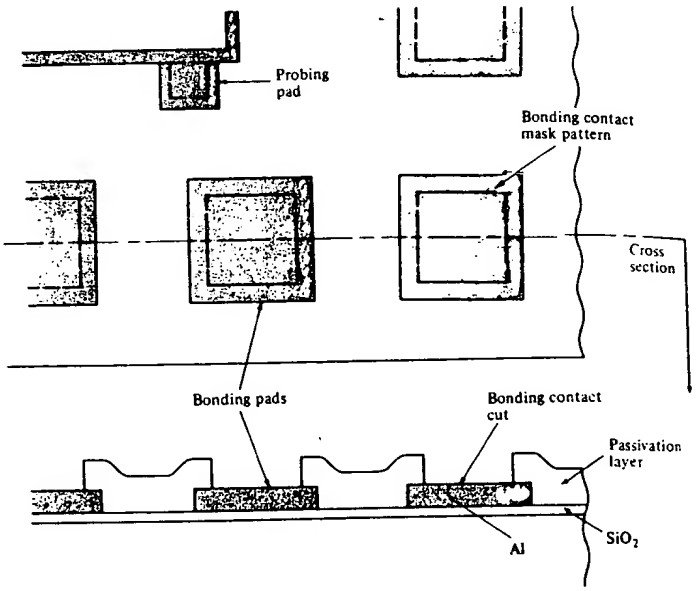



**Fig. 5-16** Passivation layer and bonding pad openings. (Note, cross-section not to scale.)

# Microchip Fabrication

## A Practical Guide to Semiconductor Processing

Peter Van Zant

Fourth Edition

McGraw-Hill

New York San Francisco Washington, D.C. Auckland Bogotá
Caracas Lisbon London Madrid Mexico City Milan
Montreal New Delhi San Juan Singapore
Sydney Tokyo Toronto

**Library of Congress Cataloging-in-Publication Data**

Van Zant, Peter.
Microchip fabrication : a practical guide to semiconductor processing / Peter Van Zant.—4th ed.
p. cm.
Includes bibliographical references and index.
ISBN 0-07-135636-3
1. Semiconductors—Design and construction. I. Title.
TK7871.85.V36 2000
621.3815'2—dc21

00-02317

*McGraw-Hill*
*A Division of The McGraw-Hill Companies*



1 2 3 4 5 6 7 8 9 0 DOC/DOC 0 9 8 7 6 5 4 3 2 1 0

ISBN 0-07-135636-3

*The sponsoring editor for this book was Stephen Chapman and the production supervisor was Sherri Souffrance. It was set in Century Schoolbook by Pro-Image Corporation.*

*Printed and bound by R. R. Donnelley & Sons Company.*

This book is printed on recycled, acid-free paper containing a minimum of 50% recycled, de-inked fiber.



*Many th*
*wife, an*
*brought*
*the dem*

layer over the metallization terminal pads on the periphery of the chip. This step is known as the *pad mask* (not shown in Fig. 4.6).

The 12-step process illustrates how the four basic fabrication operations are used to build a particular transistor structure. The other components (diodes, resistors, and capacitors) required for the circuit are formed in other areas of the circuit as the tranisitors are being formed. For example, in this sequence resistor patterns are put on the wafer at the same time as the source/drain pattern for the transistor. The subsequent doping operation creates the source/drain *and* the resistors. Other transistor types, such as bipolar and silicon gate MOS, are formed by the same basic four operations, but using different materials and in different sequences.

### Chip Terminology

Figure 4.17 is a photomicrograph of an MOS medium-scale integration (MSI) integrated circuit. This level of integration was chosen so that the surface details could be seen. The components of higher-density circuits are so small that they cannot be distinguished on a photomicrograph of the entire chip. The chip features are:

1. A bipolar transistor
2. The circuit designation number
3. Bonding pads for connecting the chip into a package
4. A piece of contamination on a bonding pad
5. Metallization lines
6. Scribe (separation) line
7. Unconnected component
8. Mask alignment marks
9. Resistor

### Wafer Sort

Following the wafer-fabrication process comes a very important testing step, wafer sort. This test is the report card on the fabrication process. During the test, each chip is electrically tested for electrical performance and circuit functioning. Wafer sort is also known as *die sort* or *electrical sort.*

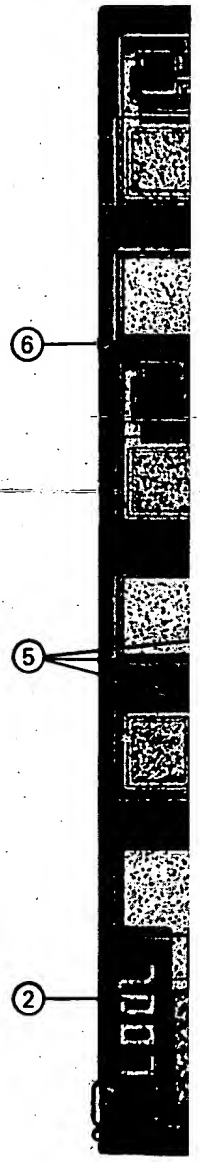



Figure 4.17 Chip t

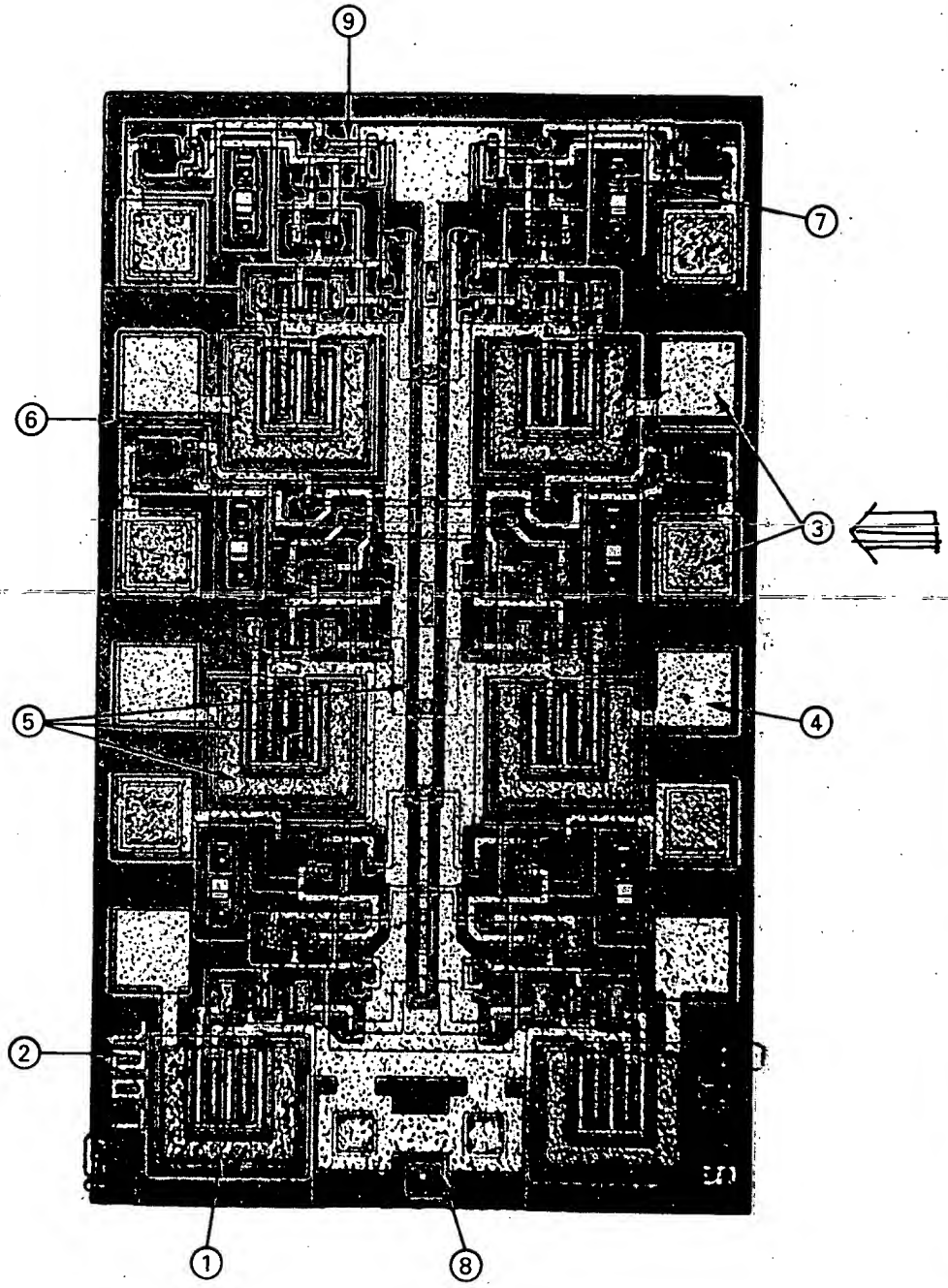



Figure 4.17 Chip terminology.

Another chip characteristic of importance to the packaging process is heat generation. Chips used in high-power circuits and highly integrated circuits can generate enough heat to actually damage themselves and the circuit. Package design includes heat dissipation factors. Heat is also an important parameter in packaging processes, with packaging process temperatures limited to 450°C. Above this temperature, the aluminum and silicon contacts on the chip can form an alloy in the wafer surface that causes electrical shorts.

## Package Functions and Design

There are four basic functions performed by a semiconductor package. They are to provide

1. A substantial lead system
2. Physical protection
3. Environmental protection
4. Heat dissipation

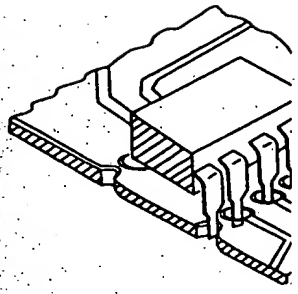
### Substantial lead system

The primary function of the package is to allow connection of the chip to a circuit board or directly to an electronic product. This connection cannot be made directly due to the thin and fragile metal system used to interconnect the components on the chip surface. The metal leads are typically less than 1.5 $\mu$m thick and often only 1 $\mu$m wide. The thinnest wires available are 0.7 to 1.0 mils in diameter, which is many times larger than the surface wiring. This difference in wiring sizes is the reason that the chip wiring terminates in the larger bonding pads around the edge of the chip.

Even though the wires are larger, at 1 mil in diameter they too are very fragile. This fragility is overcome by a more substantial electrical lead system that serves as the connection of the chip to the outside world (Fig. 18.4). The lead system is an integral part of the package.

### Physical protection

The second function of the package is the physical protection of the chip from breakage, particulate contamination, and abuse. Physical protection needs vary from low, as in the case of consumer products, to very stringent, as in the case of automobile circuits, space rockets, and military uses. The protection function is accomplished by securing the chip to a die-attachment area and surrounding the chip, wire



bonds, and inner pac
size and eventual use
the enclosure and the

### Environm ntal pr t cti

Environmental prote
gases that may interf
package enclosure.

### Heat dissipati n

Every semiconducto
Some generate larg
serve to draw the hea
in choosing a packag
chips that generate l
eration in the packa
size of the package
dissipating fins or b

### Overvi w of Packa

In this section a sir
presented.

### Cleanlin ss and stati

The vulnerability
entire lifetime. Wh
maintain the same
4), cleanliness is i
contamination con
eas, particularly, d

**ass mbly** The series of operations after fabrication in which the wafer is separated into individual chips and mounted and connected to a package.

**atmosph ric oxidation** A process of oxidation of silicon carried out at atmospheric pressure. The equipment used for thermal oxidation is the same as that used for thermal diffusion. It is composed of four subassemblies: a reactant source cabinet, a reaction chamber, a heating source, and a wafer holder.

**atomic force microscope (AFM)** A microscope for profiling wafer surfaces by plotting the output of a spring-balanced probe moved over the surface.

**atomic number** A number assigned to each element equal to the number of protons (therefore the number of electrons) in the atom.

**atomic particles** The parts of an atom: electrons, protons, and neutrons.

**base** (1) The control portion of an NPN or PNP junction transistor. (2) The P-type diffusion done using boron that forms the base of NPN transistors, the emitter and collector of lateral PNP transistors, and resistors.

**binary notation** A way of representing any number using a power of 2 (the digits 0 and 1).

**bipolar transistor** A transistor consisting of an emitter, base, and collector, whose action depends on the injection of minority carriers from the base by the collector. Sometimes called NPN or PNP transistor to emphasize its layered structure.

**bi-MOS** A circuit containing both bipolar and MOS transistors.

**boat** (1) Pieces of quartz or metal joined together to form a supporting structure for wafers during high-temperature processing steps. (2) A Teflon or plastic assemblage used to hold wafers during wet processing steps.

**boat puller** A mechanical arrangement to push a boat loaded with wafers into a furnace and/or withdraw it at a fixed speed.

**BOE** See **buffered oxide etch.**

**bonding pads** Electrical terminals on the chip (generally around the periphery) used for connection to the package electrical system.

**boron (B)** The P-type dopant commonly used for the isolation and base diffusion in standard bipolar integrated circuit processing.

**boron trichloride ($BCl_3$)** A gas that is often used as a source of boron for doping silicon.

**bubbler** An apparatus in which a carrier gas is "bubbled" through a heated liquid, causing portions of the liquid to be transported with the gas, e.g., a carrier gas (nitrogen or oxygen) is bubbled through deionized water at 98 to 99°C on its way to the oxidation tube.

**buffered oxide etch** A mix of hydrogen fluoride (HF) and ammonium fluoride ($NH_4F$) used to allow oxide etching to occur at a slow, controlled rate.